HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6402

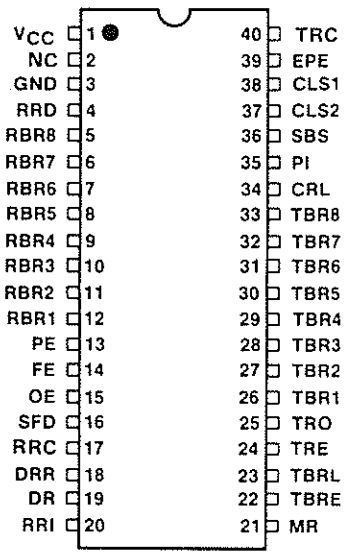
CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)

JANUARY 1978

Features

- OPERATION FROM D.C. TO 4.0MHz @10.0 VOLTS
- LOW POWER-TYP. 10mW @ 2.0MHz AND 5.0 VOLTS
- 4V TO 11 VOLT OPERATION
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UART'S
- SINGLE POWER SUPPLY

Pinout

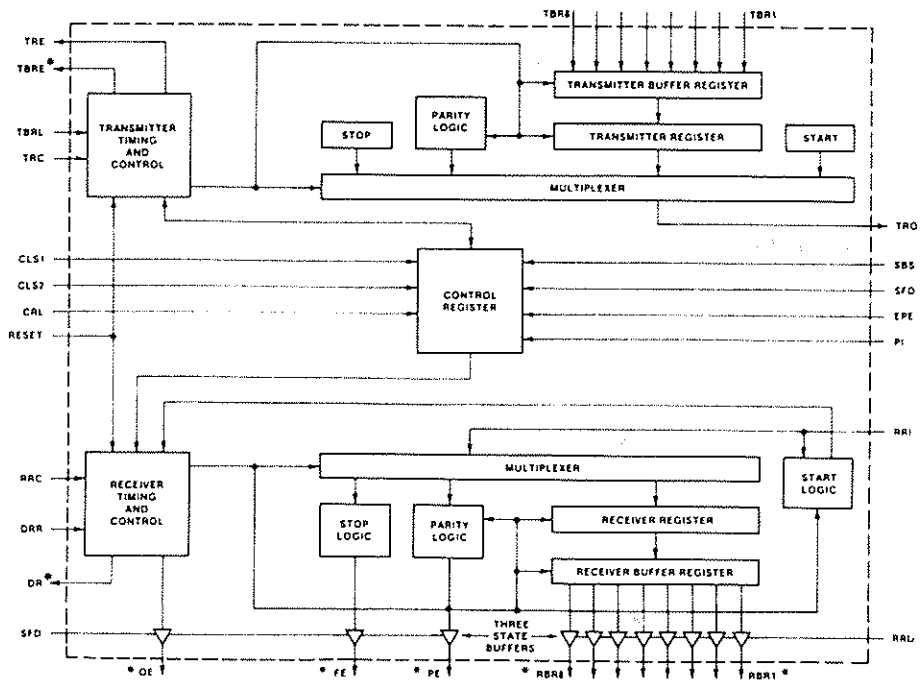


Description

The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operation clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Functional Diagram



* These outputs are three state

Control Definition

CONTROL WORD — CHARACTER FORMAT

CLS2	CLS1	PI	PE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

Specifications HD-6402A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6402A-9	-40°C to +85°C
Military HD-6402A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 10.0V ± 0.5V, TA = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% VCC			V	
V_{IL}	Logical "0" Input Voltage			20% VCC	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage*	VCC -0.01			V	$I_{OUT} = 0$
V_{OL}	Logical "0" Output Voltage*			GND +0.01	V	$I_{OUT} = 0$
I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		5.0	500	μA	$V_{CC} = 10.5V$, $V_{IN} = V_{CC}$ or GND
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		6.0	10.0	pF	

*Guaranteed but not 100% tested.

A.C.

		VCC = 10.0V ① TA = 25°C			VCC = 10V ± 0.5V TA = Industrial or Military				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		6.0	D.C.		4.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	75			100			ns	$C_L = 50pF$
t_{pw}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	40			40			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	30			30			ns	
t_{pd}	Output Propagation Delays			50			70	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

Switching Waveforms

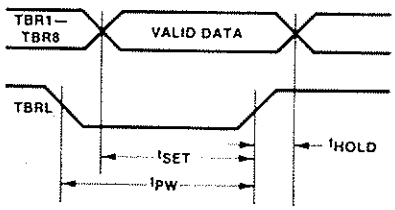


FIGURE 1
Data Input Cycle

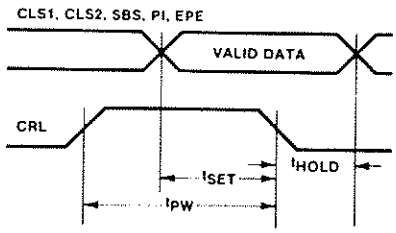


FIGURE 2
Control Register Load Cycle

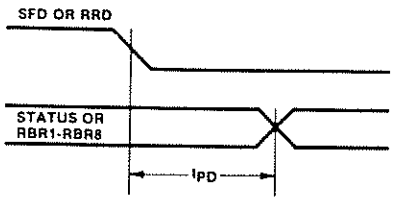


FIGURE 3
Status Flag Output Delays
or Data Output Delays

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6402-9	-40°C to +85°C
Military HD-6402-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = −0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		1.0	100	μA	V_{IN} = GND or V_{CC}; V_{CC} = 5.5V, Output Open
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested

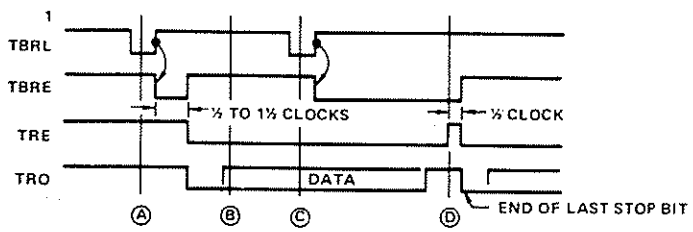
A.C.

		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		3.0	D.C.		2.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	150			150			ns	C_L = 50pF
t_{pw}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	50			50			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	60			60			ns	
t_{pd}	Output Propagation Delays			125			160	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. Ⓐ Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. Ⓑ The rising edge of TBRL clears TBREmpty. ½ to 1½ clock cycles later, data is transferred to the transmitter register; TREmpty is cleared; TBREmpty is set high; and serial data transmission is started. Output data is clocked by TRClock. The clock rate is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



TRANSMITTER TIMING (NOT TO SCALE)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range (Industrial -9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 5%, T_A = Industrial

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	V_{CC} -2.0			V	
V_{IL}	Logical "0" Input Voltage			0.8	V	
I_{IL}	Input Leakage	-10.0		+10.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = 0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-10.0		+10.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		1.0	800	μA	V_{IN} = GND or V_{CC}, V_{CC} = 5.25V, Output Open
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested.

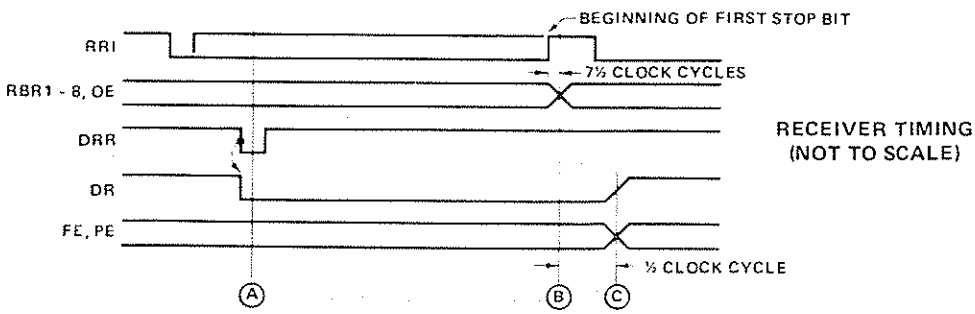
A.C.

		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ± 5% T_A = Industrial				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		2.0	D.C.		1.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	200			225			ns	C_L = 50pF
t_{pw}	Pulse Width MR	500			600			ns	See Switching Time
t_{SET}	Input Data Setup Time	60			75			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	75			90			ns	
t_{pd}	Output Propagation Delays			150			190	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Receiver Operation

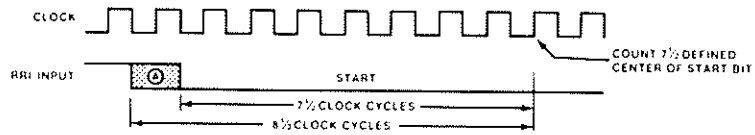
Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Ⓐ A low level on DRReset clears the DReady line. Ⓑ During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. Ⓒ ½ clock cycle later DReady is reset to a logic high, PError and FError are evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.



RECEIVER TIMING
(NOT TO SCALE)

Start Bit Detection

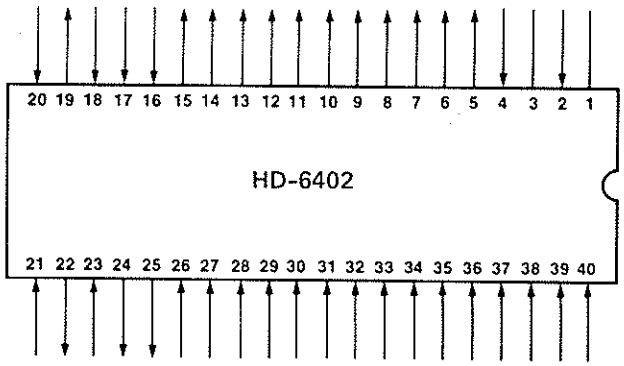
The receiver uses a 16X clock for timing. Ⓐ The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symetrical square wave, the center of the start bit will be located within ±½ clock cycle, $\pm\frac{1}{32}$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



Pin Assignment And Functions

PIN	SYMBOL	DESCRIPTION
1	VCC	Positive Voltage Supply
2	NC	No Connection
3	GND	Ground
4	RRD	A High level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1 - RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	See Pin 5 - RBR8
8	RBR5	See Pin 5 - RBR8
9	RBR4	See Pin 5 - RBR8
10	RBR3	See Pin 5 - RBR8
11	RBR2	See Pin 5 - RBR8
12	RBR1	See Pin 5 - RBR8

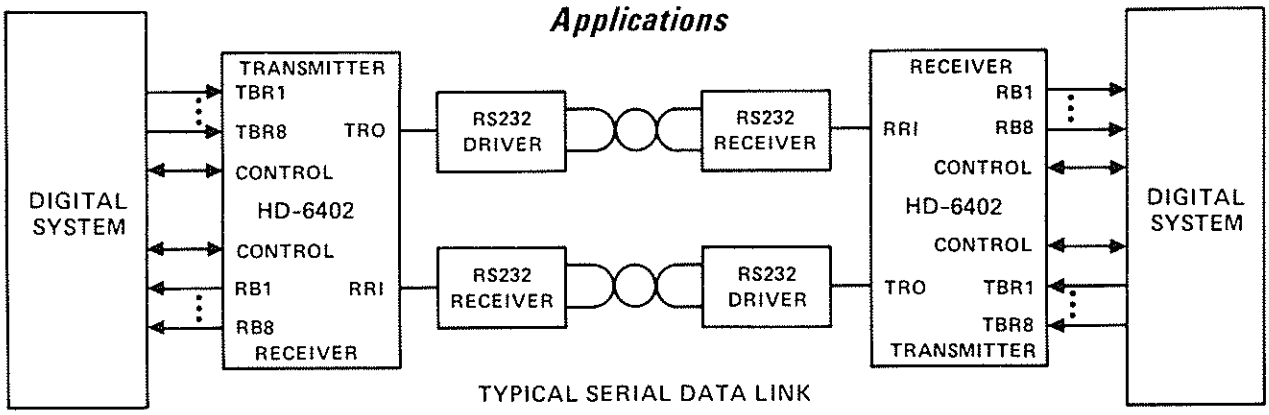
PIN	SYMBOL	DESCRIPTION
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output DR, to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.



PIN	SYMBOL	DESCRIPTION
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1 - TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1 - TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.

PIN	SYMBOL	DESCRIPTION
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation, Parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits)
38	CLS1	See Pin 37 - CLS2
39	EPE	When PI is low a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

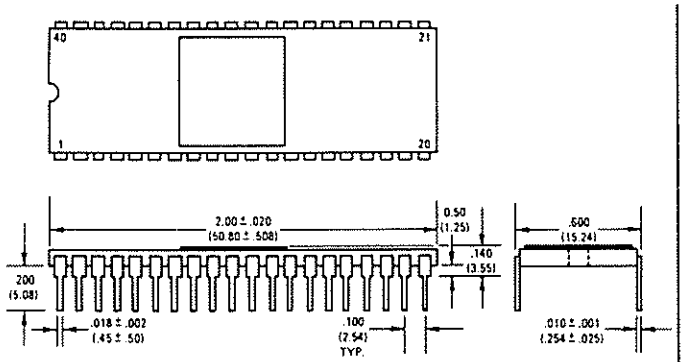
Applications



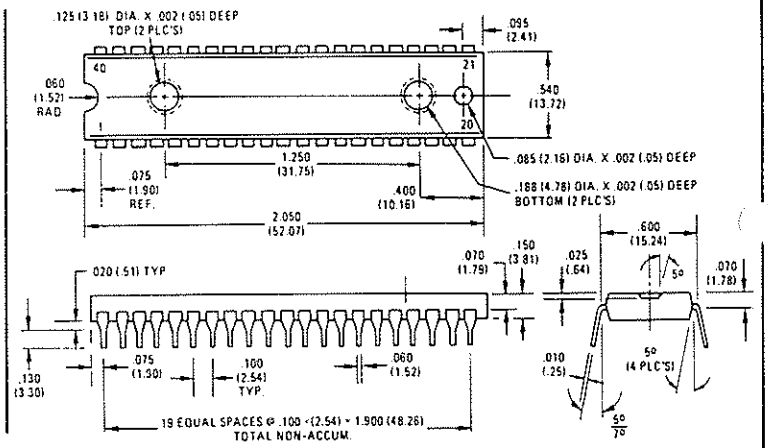
TYPICAL SERIAL DATA LINK

Packaging

40 LEAD CERDIP



40 LEAD EPOXY



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Ordering Information

HD 1 - 6402 A - 2

- HD 1 — HARRIS
- 1 — PACKAGE CODE: 1: Ceramic; 3: Epoxy
- 6402 — DEVICE NUMBER
- A — VERSION: A: 10.0V Nominal; BLANK: 5.0V Nominal; C: Relax 5.0V Nominal
- 2 — TEMPERATURE: 2: -55°C to +125°C; 8: Mil. Std. 883B; 9: -40°C to +85°C

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